sequence this D-trigger 52 is written the logical level corresponding by Usn control signal, moreover the reset after each writing (or by run) takes place by commands, they enter from PC6 through the synchronisator 7 input register 53 on the R-input of this D-trigger 52,

on the first input of the I sheme 51 enter the signal with inverse Q\-output of the D-trigger 52 and on their second input -the f1 signal with the above indicated synchro-TV generator 40 output.

So it is formed the Uc control signal, it is the sequence of theimpulses with f1 signal sequence and it provides in the interframe accumulators 14 the fragment videosignal accumulation (by low logical level of the Usn signal) and receipt of the essentially cleaning from noises of the "freezing" fragment image (by high logical level of the Usn signal).

The Manufactoring applicationity of the suggested TV high resolution TV system is caused, in first, the possibility of their manufactoring on the modern element base in the different configuration, and second, the possibility of the application for synthesis of the integrate (without visible foints) images with high resolution faculty from fragment videosignals from well regulated multitude standart TV cameras,it allow use the such system for need, for example, mapgraphy and in combination with X-ray source - for functional X-ray diagnosis needs as it in detail has been showed above.

INVENTION FORMULA

1. The high resolution TV system, having at least two TV cameras, the analog - digital convertor (ADC) block, the videosignal standart convertor, random - access memory (RAM), the output videosignal synthesis means, connected with the TV camera outputs and with each other, and the central processing unit on the PC base, it distinguished that the output videosignal synthesis means is executed on the multichannel geametric distortion corrector base and the synchronisator, by this the indicated corrector is connected through the ADC block to TV camera output and through the videosignal standart convertor and RAM - on the PC

input, and the synchronisator is connected through its control input - on the synchronization output at least one of TV cameras, and through of their control output - the clock input of the ADC block, on the address inputs of the indicated corrector and on the address and control synchronisated inputs of the videosignal standart convertor.

2. The TV system by p.1, it's distinguished that it is supplied by the primary (X-ray) source and X-ray image convertor in the visible image, they are in succession mounted before TV cameras.

3. The TV system by p.1, it's distinguished that it is supplied at least by the one calibrated test - object in form of spasing mir, it by installation may be located before TV cameras.

4. The TV system by p.3, it's distinguished that it is supplied by the calibrated test - object location means in the field of vision and removal these objects from TV camera field of vision, it is connected on the control synchronisated output of the synchronisator and this synchronisator in addition is interconnected with PC by controlling reverse connection circle.

5. The TV system by p.1, it's distinguished that it is supplied by high resolution monitor, it's connected on the information output of the videosignal standart convertor and RAM.

6. The TV system by p.1, it's distinguished that the geometric distortion multichannel corrector in each channel has:

on the input:

- at least the two identical calculator of the corrected coordinated accordingly by horisontal and vertical of each image element (pixel) in the output videosignal, calculating on the base of fnalogous pixel initial coordinates in the input videosignal and corrected coefficients, and

- at least the two identical controlled memory blocks of the input digital videosignal, connected to indicated calculators as address sources for the information reading about corrected elements of the output videosignal, and

on the output:

- the invertor, it is connected between the indicated above synchronisator and one of the indicated controlled memory block, and

- the output multiplexor for alterhated attaching of the indicated controlled memory block output on the above indicated videosignal standart convertor and RAM inputs.

7. The TV system by p.6, it is distinquished that the each indicated calculator has at least:

- the one input comparator with fixed value of the threshold digital code, connected to one of ADC output;

- the one decipherator, connected on the address outputs of the input image pixel coordinated with above indicated synchronisator and hsving the two control output,

- the two logical I shemes, each of them is connected to the indicated comparator output and to synchronisator control output and one of them is connected to first, and second - to the second control output of the indicated decipherator,

- the two nonvolatile RAM, in them:

-- the control input are independely connected to outputs of the corresponding logical I shemes and

-- the address and information input are also independely connected accordingly to adress output of the above indicated synchronisator,

- the one decipherator, connected on the one of coordinate of the input image of each pixel address output with the above indicated synchronisator (by this in the first and second nonvolatile RAM of the first calculator on their information inputs enter the signal, corresponding by one of coordinate of each input image pixel, on the address inputs same RAM enter, the signal, corresponding by second coordinate of each input image pixel, and on the corresponding inputs of the first and second nonvolatile RAM and on the decipherator of the second calculator the indicsted signals enter in the return order),

- the one difference cascade with two information input separately connected accordingly to the information output of the indicated nonvolatile RAM,

- the standartisator for integer - valued devision of the digital parallel signal code, settig the one of coordinate of each distorted image pixel, on the digital constant code, setting one of distorted raster geometric sizes (accordingly by horisontal in one and by vertical in other calculator),

- the multiplier for multiplying the one of standartisated coordinate digital codes of each input image pixel on the corresponding by this coordinate the digital code of the distorted raster following size,

- the summator for addition of the beggining distorted raster coordinate digital codes and following augment of the treating image pixel coordinate in same raster, and

the each controlled memory block has:

- the two input multiplexors, each of them is intended for forming of the corresponding input and corrected image coordinate digital codes, and connected to the indicated multiplexors

- RAM for writing by one addresses of the input videosignal and reading by other addresses of the output videosignal.

8. The TV system by p.1, it's distinquished that the indicated videosignal standart convertor is combined with indicated RAM and has:

the unbinded by the information input the RAM banks, the number of them equal the TV camera number and in each of them are included:

- the two address multiplexors and

- the two frame RAMs;

the RAM bank operation decipherator;

the first digital analog convertor;

the buffer RAM, it contains:

- the parallely connected memory blocks, the number of them equal the TV camera number and

- the buffer RAM decipherator and

the second digital analog convertor.

9. The TV system by p.8, it's distinquished that

(a) ineach of mentioned RAM bank:

the information inputs of the frame RAM are united and connected to the corresponding outputs of the indicated geometric distortion multichannel corrector, and their information outputs are also united (including - and between banks) and connected to the information input of the first digital analog convertor;

the first inputs of the multiplexors are united and connected to the synchronisated output of the corrected image writing coordinate codes in the frame RAM in the above indicated synchronisator, and the second inputs of the multiplexors are also united and connected to the synchronisated outputs of the corrected image reading coordinate codes in the frame RAM in the above indicated synchronisator;

the first outputs of the first multiplexor are connected to the corresponding inputs of the first frame RAM address and the first

outputs of the second multiplexor are connected to the corresponding inputs of the second frame RAM address;

the second control input of the first multiplexor and the second (inverse) control input of the second multiplexor are connected to the control output of the above indicated synchronisator;

the first multiplexor outputs are connected to the address inputs, the second outputs - to the control inputs of the chip selection and their third outputs - to the control reading-writing inputs of the corresponding RAM;

(b) in all RAM banks:

the first control inputs of the first and second multiplexors are united and connected accordingly to the first, second and so on decipherator outputs, and

the information outputs of all frame RAM are united and connected to the information input of the first digital analog convertor;

(c) the decipherator control input are connected to the control output of the above indicated synchronisator;

(d) the first and second control inputs of the first digital analog convertor are accordingly connected to the synchronisated output of the above indicated synchronisator, and the information output of this convertor is connected to the above indicated high resolution monitor;

(e) the address inputs of the buffer RAM memory blocks are united and connected to the synchronisated outputs of the above indicated synchronisator with the coordinate codes; their information inputs are connected to the corresponding outputs of the above indicated geometric distortion multichannel corrector; their reading-writing operation inputs are connected to the control output of the above indicated synchronisator and the information input of the last memory block of the indicated buffer RAM is connected to the corresponding information input of the frame RAM;

(f) the decipherator control input of the buffer RAM are connected to the corresponding control outputs of the above indicated synchronisator, and the control outputs of the indicated decipherator are connected to the chip selection inputs of the memory blocks so, that the first of the indicated outputs is connected with the indicated inputs of the first memory block, the

second - with the input of the second memory block and so on;

(g) the information input of the second digital analog convertor is connected to the united information outputs of the memory blocks, the control inputs of this convertor are accordingly connected to the synchronisated outputs of the above indicated synchronisator and their information output is connected to the above indicated videosignal entering in the PC 3 block.

10. The TV system by p.1, it's distinquished that the synchronisator has:

the first setting synchronisating signal generator, corresponding of it is connected to the clock inputs of the above indicated ADC blocks and multichannel threshold control device and

at least the one second setting synchronisating signal generator, corresponding by the synthesated image high resolution standart;

the two meter groups accordingly for X and Y coordinates of the image pixels, forming by each TV camera, and

the two meter groups accordingly for Xm and Ym coordinates of the high resolution synthesater image pixels;

at least the one synchroimpulse selector, intended for separating from full TV signal of the initial synchronisating impulses and forming of the output horisontal and vertical synchronisating impulses;

the two digital comparator accordingly for Xm and Ym coordinate codes;

the two one-vibrators for forming of the horisontal (line) and vertical (frame) impulses corresponding by high resolution standart;

at least the one high resolution synthesated image pixel number meter;

the I sheme for conjunction by forming of the control signals for the above indicated geometric distortion corrector;

the input register for reception by the indicated synchronisator the control commands, entering from the indicated PC;

the output register for giving the information about the indicated synchronisator state in the indicated PC and

the address decipherator by programmely forming port of the indicated PC for giving in the indicated synchronisator the control commands,

by this:

the first setting generator is connected to the accounting input of the first X coordinate meter group;

the accounting input of the second Y coordinate meter group is connected to the horisontal synchronisating impulse output of the synchroimpulse selector;

the first Xm coordinate meter group is connected by the accounting input to the second setting synchronisated signal generator output;

the accounting input of the second Ym coordinate meter group is connected to the Xm coordinate meter output through in succession connected one of the digital comparators and one of the one-vibrators;

the reset inputs of the first X coordinate meter group and the first Xm coordinate meter group are connected to the horisontal synchronisating impulse output of the synchroimpulse selector;

the reset input of the second Y coordinate meter group is connected to the same synchroimpulse selector output, with it must be taken off the vertical synchronisating impulses corresponding by the full frame of the TV camera output image;

the reset input of the second Ym coordinate meter group is connected to the same synchroimpulse selector output, with it must be taken off the vertical synchronisating impulses corresponding by the half frame of the TV camera output image;

the first Xm coordinate meter group output is connected:

- to the inputs of all multiplexors and on the RAM bank operation decipherator input of the above indicated videosignal standart convertor with RAM and

- through in succession connected the first digital comparator and the first one-vibrator - to the digital analog convertor of same convertor with RAM, and also

- to the accounting input of the second Ym coordinate meter group;

the second Ym coordinate meter group output is connected:

- to the inputs of all multiplexors of the above indicated videosignal standart convertor with RAM and

- through in succesion connected the secong digital comparator and the second one-vibrator - to the digital analog convertor of same convertor with RAM, and also

- to the accounting input of the high resolution synthesated

image pixel number meter;

the input register is connected:

- by parallel data entering - to the PC,

- by first output - to the reset input of the high resolution synthesated image pixel number meter and the control input of the the videosignal standart convertor with RAM,

- by second output - to the second input of the I sheme;

- by third output - to the reset input of the D-trigger;

the output register is connected:

- by first input - to the vertical synchronisating impulse output of the above indicated synchroimpulse selector,

- by second input - to the output of the high resolution synthesated image pixel number meter, and

- by output - to the PC;

the address decipherator by programmely forming PC port for giving in the above indicated control command synchronisator is connected:

- by input - to the PC address bus, and

- by output - to the input register input;

the high resolution synthesated image pixel number meter in addition is connected on the control input of the buffer RAM decipherator of the above indicated videosignal standart convertor with RAM.

11. The TV system by p.10, it's distinguished that the synchronisator is, in addition, supplied by the second I sheme and D-trigger, moreover:

the indicated I sheme by one input is connected to the setting synchronisating signal generator output corresponding by TV camera resolution standart, by second input - to the inverse output of the D-trigger and the output may be used in the additional forming input signal circle for the above indicated geometric distortion corrector, and

the indicated D-trigger is connected:

- by information input - to the control output of the the above indicated multichannel threshold control device,

- by synchronisated input - to the synchroimpulse selector output corresponding by a whole frame of the input image,

- by reset input - to the third output of the above indicated input register.

12. The TV system by p.10, it's distinguished that it's, in addition, supplied by the digital videosignal amplitude corrector, it is connected on the geometric distortion multichannel corrector input by interframe accumulators of the difital videosignals, the number of theirs usually equal the TV camera number and they are connected between ADC block and the indicated digital videosignal amplitude corrector and multichannel threshold control device, it's connected on the digital videosignal amplitude corrector outputs through the above indicated synchronisator is connected to the control inputs of the digital videosignal interframe accumulators and supplied by control outputs of the reverse connection with the primary (X-ray) source.

13. The TV system by p.12, it's distinguished that the digital videosignal amplitude corrector is executed by multichannel and in each channel has:

the two nonvolatile RAM, they are accordingly intended for saving of the "black" level corrected coefficient codes and maximum videosignal range for each pixel of the input image from corresponding (by given channel) TV camera;

the difference cascade for difference calculation of the input signal and "black" level codes for each pixel of the input image from corresponding TV camera;

the devisor for amplitude correction standarted coefficient calculation of the input videosignals by division the constant setting for chosen TV cameras and ADC the maximum videosignal range code, on the alternating code, corresponding by the maximum videosignal range for each following pixel of the input image from corresponding TV camera;

the address decipherator by programmely forming PC port for giving control commands in the given channel of the the digital videosignal amplitude corrector, in it the input is connected to the PC address bus;

the input register for reception of the contol commands, entering from PC, in it:

- the first input is connected to the PC data bus, the second input - to the address decipherator output, and

- the outputs are connected to the control inputs of the nonvolatile RAMs;

the output multiplier for forming of the standartisated output

videosignal codes by multiplying of the mentioned standartisated coefficients on the mentioned difference signal code,

moreover:

the first RAM is connected:

- by information input - to the output of the corresponding channel of the above indicated ADC block,

- by control input - to the first output of the input register,

the second RAM is connected:

- by information input - to the output of the above indicated difference cascade,

- by control input - to the second output of the input register, and

by address inputs both RAMs are connected to the X,Y outputs of the above indicated synchronisator;

the difference cascade is connected:

- by first input - to the output of the corresponding channel of the above indicated ADC block,

- by second input - to the output of the first RAM,

- by output - on the first input of the indicated multiplier;

the divisor is connected between the output of the second RAM and the second multiplier input.

14. The TV system by p.12, it's distinguished that the multichannel threshold control device has:

in each channel:

- the first comparator for comparison of the image pixel codes forming by corresponding given channel the TV camera with the threshold code,

- the I sheme, it by first input is connected to the comparator output and intended for strobition of the clock signal by output signal of this comparator,

- the meter, the accounting input of it is connected to the indicated I sheme output and it serves for such pixel number calculation in the image frame corresponding by connected to the given channel the TV camera, their code exceed the setting threshold brightness value,

- the register, it information input is connected to the meter output and it serves for the parallel output code saving of this meter,

- the second comparator, it input through the indicated

register is connected to the indicated meter output and it serves for comparison of this meter output code and setting threshold image pixel number having the brightness none less mentioned threshold value, and

- the trigger, it information input is connected to the indicated comparator output and it serves for the logical output signal of this comparator writing by synchronisating frame impulse end from the above indicated synchronisator; and

the common for all channels:

- the address decipherator of the programmely forming PC port for giving in the multichannel threshold control device of the threshold brightness value codes, the pixel number with brightness none less the threshold value and channel number with "1" logical level on the outputs, in it the input is connected to the PC address bus,

- the input register takes the indicated threshold values entering from PC, in it the first (information) input is connected to the PC data bus and the second (clock) input - to the address decipherator output, the first output (threshold brightness value code) is connected to the united first inputs of the first comparators of all channels,

- the multiplexor for multipletion of the output signals of all channels, in it each information input is connected to the trigger outputs of corresponding channels and the control input - to the synchronisating output of the above indicated synchronisator with X coordinate code;

- the I sheme for strobition of the clock signal by the output signal of the indicated multiplexor, in it the first input is connected to the multiplexor output, and the second input is connected to the united second inputs of the indicated I shemes of each multichannel threshold control device channels and connected to the clock output of the above indicated synchronisator;

- the meter for such channel number calculation, the signals on their trigger outputs have the "1" logical level and it is connected by accounting input - to the indicated I sheme output and by reset input through the invertor - to the synchronisating frame impulse output of the above indicated synchronisator,

- the comparator for comparison of the meter output code and threshold value of the channel number with "1" logical level on the

outputs connected by the first and second information inputs accordingly to the meter output and to the third output of the indicated input register and by output - to the primary (X-ray) source controller,

- the trigger for writing and saving of the indicated comparator output signal connected by the information input - to the indicated comparator output, by the clock input through the indicated invertor - to the synchronisating frame impulse output of the above indicated synchronisator and by the information output - to the above indicated interframe accumulators through the above indicated synchronisator,

by this

in each channel is united and in common connected to the synchronisating frame impulse output of the above indicated synchronisator:

- the reset inputs of the pixel number meters with brightness none less of the setting value,
- the clock inputs of all registers and
- the clock inputs of all triggers, and

the first comparator second inputs of all channels are connected to the correspinding information outputs of the above indicated digital videosignal amplitude corrector.

==========

P A P E R

HIGH RESOLUTION TV SYSTEM has at least the two TV cameras, the analog digital convertors (ADC) block, the videosignal standart convertor, random-access memory (RAM), the output vidrosignal sunthesis means connected with TV camera outputs and with each other, and central processing unit on the PC base. For efficient "sewing" of the separare images in the integrate (excluding the "joints") picture of the dynamical process it's characterise by the resolution none less 3000x4000 elements with legiblity and contrast none worse then in the images on the wide format X-ray photo- and cine film, the output videosignal synthesis means on the geometric distortion multichannel corrector and synchronisator bases, by this the indicated corrector is connected through the ADC